Application No. 10/583,397
Reply to Office Action dated 09/08/2010

Amendments to the Drawings:

The attached sheets of drawings includes a change to Fig. 7. Sheet 5 of 6, which includes Figs. 7 and 8, replaces the original sheet including Figs. 7 and 8.

In amended Fig. 7, the word "bugger" has been revised to "buffer" to correct the typographical error.

Attachment: Replacement Sheet (1 sheet)

REMARKS

Applicant respectfully requests favorable reconsideration and reexamination of this application. The drawings and specification have been revised editorially. Claims 1, 6, 8-11 and 13 have been revised editorially. Claim 13, which is indicated as allowable, has also been rewritten in independent form. Claims 1-13 remain pending in the application.

Objections to the Drawings

The drawings are objected to due to informalities. Fig. 7 has been revised editorially to address the Examiner's concern. Withdrawal of the objection is respectfully requested.

Objections to the Specification

The specification is objected to due to informalities. The specification has been revised editorially to address this issue. Withdrawal of the objection is respectfully requested.

Claim Objections

Claim 13 is objected to due to informalities. Claim 13 has been revised editorially to address the Examiner's concerns. Withdrawal of the objection is respectfully requested.

Claim Rejections – 35 USC § 112

Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claims 1, 6, 8-11 and 13 have been revised editorially to address the issues.

In addition, with respect to the rejection concerning the term "i960-like," page 1, lines 22-24 of the specification provides that "i960 is a series of microprocessors provided by Intel Company for the embedded applications, and there are a lot of interface devices right now based upon i960 or i960-like bus interface protocol." One skilled in the art would understand that an "i960-like" interface means an interface based on the i960 or i960-like bus interface protocol. Therefore, Applicant respectfully submits that the term "i960-like" is definite.

Withdrawal of the rejections is respectfully requested.

Claim Rejections 35 USC § 103

Claims 1 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lupien Jr. et al. (U.S. Patent No. 6,996,659) in view of Ezzet (U.S. Patent No. 5,603,051). Applicant respectfully traverses this rejection.

Claim 1 requires a main controller for accomplishing bus protocol conversion between an AHB interface and an i960-like interface. Claim 1 also requires an i960-like interface including 1) a bus interface multiplexing request module for generating bus interface multiplexing request signal; and 2) a bus multiplexing module for accomplishing the multiplexing between an address bus for outputting from AHB to i960-like and a data bus for outputting from AHB to i960-like.

This arrangement allows an operation mode in which the AMBA AHB bus is used and an operation mode in which the i960-like bus is used to communicate effectively with each other.

Lupien Jr. et al. fail to teach or suggest the main controller for accomplishing bus protocol conversion between an AHB interface and an i960-like interface, as required by claim 1. Instead, Lupien Jr. et al. merely discuss a bridge core for coupling two or more busses including embedded processor busses (See Lupien Jr. et al., col. 2, lines 22-39). However, the Lupien Jr. et al. embedded processor busses cannot be simply be relied on as suggesting an AMBA AHB bus and an i960-like bus. More specifically, Lupien Jr. et al. only provide a general bus bridge architecture, which is used to solve the problem that the bridge designed for a special bus cannot be multi-functioned. In fact, the problem solved by Lupien Jr. et al. is different from the one being solved by the invention of claim 1. Lupien Jr. et al. discuss that the architecture of a bus converter can be designed as shown in Fig. 1 for the conversion between different busses, but fail to teach or suggest logical circuit structures for connecting the busses. For example, Fig. 1 of Lupien Jr. et al. merely illustrates that an ABH bus can be converted to a PCI-X bus without mentioning the specific logical circuit structure regarding how the ABH bus is converted to the PCI-X bus by the bridge 100. In fact, the bridge 100 in Lupien et al. is merely a general bridge and does not suggest the structure of a main controller as required by claim 1. Therefore, Lupien Jr. et al. provide no teachings or suggestions of how to communicate a specific bus protocol with another specific bus protocol.

Moreover, Fig. 10 of Lupien Jr. et al. merely discusses the conversion of an AHB bus to a PCI-X bus, but are silent as to a device in which an AHB bus is converted to an i960-like bus. More specifically, since the logical circuit structure of a PCI-X bus is different from the logical

circuit structure of an i960-like bus, e.g., significant difference exists in signal and timing definitions between the two type busses, the logical circuit structure of the PCI-X bus cannot be simply relied on as suggesting the logical circuit structure of an i960-like bus. Therefore, one skilled in the art would not be able to modify the conversion between an AHB bus and a PCI-X bus to arrive at the invention of claim 1.

Ezzet does not remedy the deficiencies of Lupien Jr. et al. Ezzet merely discusses an I/O processor with a local memory providing shared resources for a plurality of I/O interfaces on an I/O bus, where a block diagram of an implementation of an I/O processor 113 is illustrated (see Ezzet, Fig. 5). Ezzet also discusses a device in which an I/O processor is used with an i960 bus standard, but is silent as to the specific structural elements of the i960 bus. For example, Ezzet provides no teachings or suggestions of 1) a bus interface multiplexing request module used for generating a bus interface multiplexing request signal, and 2) a bus multiplexing module used for accomplishing multiplexing between an address bus for outputting from AHB to i960-like and a data bus for outputting from AHB to i960-like, as required by claim 1.

For at least these reasons, claim 1 is patentable over Lupien Jr. et al. in view of Ezzet. Claims 6-9 depend ultimately from claim 1 and are patentable along with claim 1 and need not be separately distinguished at this time. Applicant is not conceding the relevance of the rejection to the remaining features of the rejected claims.

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lupien Jr. et al. (U.S. Patent No. 6,996,659) in view of Ezzet (U.S. Patent No. 5,603,051) and further in view of Jahnke et al. (U.S. Patent No. 6,829,669). Applicant respectfully traverses this rejection. Claims 2 and 3 depend ultimately from claim 1 and are patentable over Lupien Jr. et al. in view of Ezzet and Jahnke et al. for at least the same reasons discussed above regarding claims 1 and 6-9. Jahnke et al. do not remedy the deficiencies of Lupien Jr. et al. and Ezzet. Applicant is not conceding the relevance of the rejection to the remaining features of the rejected claims.

Claim 4 depends ultimately from claim 1 and is patentable over Lupien Jr. et al. in view of Ezzet and Jahnke et al. for at least the same reasons discussed above regarding claims 1 and 6-9. Jahnke et al. do not remedy the deficiencies of Lupien Jr. et al. and Ezzet. In addition, claim 4 requires that the AHB bus write buffer module have an enabling port, and can set the size of buffering fields for the address field and data field of the AHB bus write buffer module via AHB

bus. This arrangement allows the processor connected with the AHB bus to complete writing data with a high speed to the i960-like bus, and turn to process other instructions with a high speed, without being restricted by the relatively low speed of the i960-like bus clock. As a result, the AHB bus write buffer module helps enhance the efficiency of the system connected with the AMBA AHB bus and i960-like bus. The references of record fail to teach or suggest that the AHB bus write buffer module have an enabling port, and can set the size of buffering fields for the address field and data field of the AHB bus write buffer module via AHB bus, as required by claim 4. Applicant is not conceding the relevance of the rejection to the remaining features of the rejected claim 4.

Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lupien Jr. et al. (U.S. Patent No. 6,996,659) in view of Ezzet (U.S. Patent No. 5,603,051) and further in view of Stewart (U.S. Patent No. 6,789,153). Applicant respectfully traverses this rejection. Claims 5 and 12 depend ultimately from claim 1 and are patentable over Lupien Jr. et al. in view of Ezzet and Steward for at least the same reasons discussed above regarding claims 1 and 6-9. Steward does not remedy the deficiencies of Lupien Jr. et al. and Ezzet. Applicant is not conceding the relevance of the rejection to the remaining features of the rejected claims.

Claims 10 and 11 area rejected under 35 U.S.C. 103(a) as being unpatentable over Lupien Jr. et al. (U.S. Patent No. 6,996,659) in view of Ezzet (U.S. Patent No. 5,603,051) and further in view of Fuke (U.S. Patent No. 7,165,184). Applicant respectfully traverses this rejection. Claims 10 and 11 depend ultimately from claim 1 and are patentable over Lupien Jr. et al. in view of Ezzet and Fuke for at least the same reasons discussed above regarding claims 1 and 6-9. Fuke does not remedy the deficiencies of Lupien Jr. et al. and Ezzet. Applicant is not conceding the relevance of the rejection to the remaining features of the rejected claims.

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In view of the above, it is submitted that the application is in condition for allowance. Reconsideration and reexamination are requested. Allowance of claims 1-13 at an early date is solicited. Any questions regarding this communication can be directed to the undersigned attorney, Rong Yang, Limited Recognition No. L0279 at (612) 455-3816.

Respectfully submitted,

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Dated: December 8, 2010

By: _____
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